

What is claimed is:

- 1     1.     Apparatus comprising:  
2             a main memory;  
3             an information processor operatively coupled to said main memory and  
4     having (a) a normal-operation mode in which coherence control is performed for  
5     making data in a cache memory of a processor identical to data in a main memory  
6     and (b) a power-saving mode in which coherence control is suppressed to lower the  
7     power consumption from the power consumption of the processor when in said  
8     normal-operation mode, said processor entering said normal-operation mode when  
9     an input/output device accesses main memory while said processor is in said  
10    power-saving mode;  
11            an attribute setting module for setting a device area of said main memory to  
12    a non-cacheable attribute for exempting said device area from coherence control  
13    even in said normal-operation mode, said device area being the area accessed by  
14    the input/output device of said information processor; and  
15            an operation mode setting module for allowing said input/output device to  
16    access said device area while keeping the operation mode of said information  
17    processor in said power-saving mode when said input/output device requests  
18    access to said device area in said power-saving mode.
- 1     2.     Apparatus according to claim 1, wherein if a device different from said  
2     input/output device accesses an area in said memory that is set to a cacheable  
3     attribute requiring said coherence control in said normal-operation mode, said  
4     operation mode setting module changes the operation mode of said information  
5     processor to the normal-operation mode.

1     3.     Apparatus according to claim 1, wherein when said processor receives in  
2     said power-saving mode an access request signal provided from said input/output  
3     device to access said main memory, said processor changes the operation mode  
4     of said information processor to said normal-operation mode, and said operation  
5     mode setting module invalidates said access request signal to allow said  
6     input/output device to access said device area while keeping the operation mode  
7     of said information processor in said power-saving mode.

1     4.     Apparatus according to claim 3, further comprising:  
2             a register module for associating each of a plurality of pieces of mask data  
3     with each of a plurality of input/output devices and storing said mask data, said  
4     mask data specifying whether or not said access request signal received from each  
5     of said input/output device is invalidated;  
6             a masking module for obtaining said access request signal for each  
7     input/output device and masking said access request signal with said mask data  
8     being associated with said input/output device and stored in said register module;  
9     and  
10            an input module for inputting the input signal masked by said masking  
11    module into a processor to change the operation mode of said information  
12    processor;  
13            wherein said operation mode setting module associates mask data ..  
14    invalidating said access request signal with said input/output device accessing said  
15    device area and stores said mask data in said register module to allow said  
16    input/output device to access said device area while keeping the operation mode  
17    of said information processor in said power-saving mode.

1     5.     A program for causing a computer to function as an information processor  
2     having a normal-operation mode in which coherence control is performed for  
3     making data in a cache memory of a processor identical to data in a main memory  
4     and a power-saving mode in which said coherence control is suppressed to lower  
5     the power consumption from power consumption in said normal-operation mode  
6     and entering said normal-operation mode when an input/output device accesses  
7     said main memory in said power-saving mode, said computer being caused to  
8     function as:

9             an attribute setting module for setting a device area of said main memory to  
10    a non-cacheable attribute for exempting said device area from said coherence  
11    control even in said normal-operation mode, said device area being the area  
12    accessed by the input/output device of said information processor;

13            an operation mode setting module for allowing said input/output device to  
14    access said device area while keeping the operation mode of said information  
15    processor in said power-saving mode when said input/output device requests  
16    access to said device area in said power-saving mode.

1     6.     The program according to claim 5, wherein when said processor receives in  
2     said power-saving mode an access request signal provided from said input/output  
3     device to access said main memory, said processor changes the operation mode  
4     of said information processor to said normal-operation mode; and said operation  
5     mode setting module invalidates said access request signal to allow said  
6     input/output device to access said device area while keeping the operation mode  
7     of said information processor in said power-saving mode.

1     7.     A storage medium on which the program according to claim 5 or 6 is stored.

1     8.     A control circuit for controlling mode selection in an information processor  
2     having a normal-operation mode in which coherence control is performed for  
3     making data in a cache memory identical to data in a main memory and a  
4     power-saving mode in which said coherence control is suppressed to lower the  
5     power consumption from power consumption in said normal-operation mode and  
6     entering said normal-operation mode when an input/output device accesses said  
7     main memory in said power-saving mode, comprising:  
8         a register module for storing mask data for each input/output device, said  
9     mask data indicating whether or not an access request signal provided by each of a  
10    plurality of input/output devices for accessing said main memory is invalidated;  
11         a masking module for obtaining said access request signal for each  
12    input/output device and masking said access request with mask data associated  
13    with said input/output device and stored in said register module; and  
14         an input module for entering a signal masked by said masking module into a  
15    processor to switch the operation mode of said information processor.